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Methodology, Tools and Demonstration of MCM System Optimization

Final Report

Paul D. Franzon, Ph.D.

July 31, 1997

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North Carolina State University

Abstract

Thin film/solder-bump packaging can be used to improve integrated circuit performance and cost. In this project we (1) designed and built a DES chip to demonstrate the advantages and (2) developed design methodology to support this design style, including appropriate CAD tools.

Statement of Problem Studied

Current chip design styles fail to exploit the packaging to improve cost/performance. By greatly improving the cost and density of off-chip interconnect, thin film MCM-D and flip-chip solder bump technology have the potential to improve the performance and cost. The questions that must be answered to address this potential are as follows:

- To what extent can the performance be improved through the use of this technology
- What design styles are needed to address these issues?
- What are the potential problems and barriers to implementation and how are they overcome?
- What design methodology and CAD tools are needed to support this design approach?

Summary of Most Important Results

We designed and fabricated a 3-chip, 9.6 Gbps (i.e. OC-12 rates), triple-DES encryption multichip module. (The chips have been delivered but the MCM substrate is still in manufacture due to delays at MIDAS and MMS). On these chips, the MCM substrate was used for global power, ground and clock distribution. As a result it had the following advantages over conventionally designed chips:

- It is 150 ps faster due to reduced clock skew
- It is 35% smaller due to power/ground metalization savings

We found that this 0.5 µm technology chip optimally exploited the 250 µm solder bump pitch available to us. In comparison, a 0.18 µm technology chip would need an 80 µm solder bump pitch to gain the same advantages. The packaging technology needs to scale with the semiconductor process.

As a vehicle to ensure that noise issues don't negatively impact performance, the on-MCM power, ground and clock circuits, we designed and built a noise measurement circuit; A 9-chip MCM. This MCM is still in manufacture. Modeling and simulation results indicate little in the way of deleterious noise models.

We designed a partitioned 6-issue superscaler MIPS processor, at the behavioral Verilog (HDL) level. We partitioned it into three chips - CPU, Instruction

Cache and Data Cache. The largest partition in terms of pin count was the CPU - Instruction Cache partition (at 228 pins). Breaking out and routing these lines on the chip and MCM increased the instruction fetch delay by over 500 ps. In compensation, the cache chip itself can operate 2 ns faster if built and designed in an optimized SRAM process, instead of a logic process. We also investigated architectures that reduced the delay to 250 ps. Though potentially beneficial, a big problem with partitioned architectures is the extra expense in testing. New test approaches are needed for the technology to work.

We developed a new technique for timing debug of flip-chip designs. The technique uses a special test fixture to sense the timing at a large number of access points on the surface of the chip.

We developed a partitioning tool to help in partitioning multi-chip designs. Given as input, a module-level description of the design, and a set of timing constraints, it produces a partition and floorplan that meets the timing constraints and is routable while minimizing implementation cost.

Finally, we developed a tool that automatically converts Spice files to IBIS files. IBIS is a de-facto standard for simulation of chip I/O circuits.

List of Publications

P. Franzon, Andrew Stanaski, Yusuf Tekmen, Sanjeev Banerjia,
'System Design Optimization for MCM-D/Flip-Chip,'
IEEE Trans. on Components Packaging and Manufacturing Technology,
Feb. 1996.

S. Lipa, M.B. Steer, A.C. Cangellaris and P.D. Franzon,
'Experimental Characterization of Transmission Lines in Thin-Film Multichip Modules,'
IEEE Trans. on Components Hybrids and Manufacturing Technology,
Feb. 1996.

P. Franzon, 'Multichip Module Technology,'
in the The Electronic Handbook, J. Whitaker (editor), (CRC Press), 1995.

S. Mehrotra and P. Franzon, `Performance Driven Global Routing and Wiring Rule Generation for High Speed PCBs and MCMs,' to appear in Advanced Routing of Electronic Modules, M. Pecht (editor), (Kluwer), 1995.

Toby Schaeffer, Alan Glaser, Steve Lipa and Paul Franzon, 'MCM Implementation of a Data Encryption Standard (DES) Processor,'
in the Proceedings 1997 IEEE MCM Conference.

Wes Hansford, Jennifer Peltier, Paul Franzon, Steve Lipa, and Jonathan Schaeffer,
'MIDAS Flip-Chip Service,' in the Proceedings of the 1997 IEEE MCM Conference.

Paul D. Franzon, Tom Conte, Sanjeev Banerjia, Alan Glaser,
Steve Lipa, Toby Schaffer, Andrew Stanaski and Yusuf Tekmen,
'Computer Design Strategy for MCM-D/Flip-Chip Technology',
in Proceedings 1997 Topical Meeting on Electrical Performance of Electronic Packaging.

Christoforos Harvatis, Yusuf C. Tekmen, Grif L. Bilbro, Paul D. Franzon, 'Pin Assignment for High-Performance MCM Systems', in Proceedings 1996 IEEE ISCAS Conference.

P. Franzon, 'Computer Design Strategy for MCM-D/Flip-Chip Technology,' (**Invited paper**), in Proceedings 1996 ASIC Conference.

P. Franzon, 'System Design Optimization With Multichip Module Technology,' (**Invited Paper**), in Proceedings 1996 Conference of the Brazilian Microelectronics Society.

Sanjeev Banerjia, Alan Glaser, Christoforos Harvatis, Steve Lipa, Real Pomerleau, Toby Schaffer, Andrew Stanaski, Yusuf Tekmen, Grif Bilbro, and Paul Franzon, 'Issues in Partitioning Integrated Circuits for MCM-D/Flip-Chip Technology,' in Proceedings 1996 IEEE MultiChip Module Conference.

P. Franzon, 'Optimal System Design with MultiChip Module Technology,' (**Invited Paper**), in Proceedings of Microeletronics'95.

Sharad Mehrotra, Paul Franzon, Michael Steer, `Performance Driven Global Routing and Wiring Rule Generation for High Speed PCBs and MCMs,' in Proceedings 1995 Design Automation Conference.

List of Participating Scientific Personnel and Advanced Degrees Earned

Faculty:

Paul D. Franzon, PhD
Griff Bilbro, PhD
Michael Steer, PhD

Graduate Research Assistants:

Sharad Mehotra, PhD, December 1995
Chris Havartis, PhD, May 1997

Alan Glaser, will finish his PhD in late 1998
Steve Lipa, will finish his PhD in late 1997
Real Pommerleau, will finish his PhD in late 1998
Jonathon Schaeffer, will finish his PhD in late 1997
Andrew Stanaski, will finish his PhD in late 1997
Yusuf Tekmen, will finish his PhD in early 1998

Report of Inventions

Capacitive Probe For Flip-Chip Debug, Stanaski and Franzon

Technology Transfer

There has been significant interest in our DES technology developed as part of that research. We are currently submitting a proposal to DOE and the NSA in conjunction with Secant Inc., a start-up company in Research Triangle Park, NC.

We have developed considerable interaction with member of the SHOCC program and with a number of MCM and Workstation companies, especially MMS, Sun Microsystems, and SGI. In particular, we are influencing the technology direction in the SHOCC program and with MMS (MicroModule Systems).

The Spice to IBIS converter program written as part of this effort has been distributed to over 20 companies and is in wide use. By request, we have ported it to a number of different platforms and Spice programs.